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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,294	03/26/2004	Derrick Sai Tang Butt	02-6036/L13.12-0230	9302

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,294	BUTT ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-14 and 16-18* is/are rejected.

7)☒ Claim(s) *5 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/810,294 filed on 03/26/2004. Claims 1-18 remain pending in the application.

Claim Objections

1. Claim 1 is objected to because following informalities:

line 16, Applicant must clarify what is "the nets" (said IO signal nets?);

line 18 Applicant must clarify what is "macro cell signal slots" (said macro cell IO signal slots?).

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 7-12 and 17-18 are rejected under 35 U.S.C. 102(e) as being unpatentable by Dahl (US Patent 6,734,046).

3. As to claims 1, 8 and 17 Dahl discloses:

(1) A macro cell for an integrated circuit design having an input-output (I0) region with a plurality of I0 buffer cells physically dispersed with other cells in I0 slots along an interface portion of the I0 region, the macro cell comprising:

a plurality of macro cell I0 signal slots that are physically dispersed so as to substantially align with the I0 buffer cells (To address a very tight skew specification, a macro is created in which the edge logic is placed and routed. The macro is then placed in the edge logic area in the same position with respect to respective I/O cells and will satisfy even the tightest skew constraints. In this way, both the placement and routing are tightly controlled – col.14, ll.49-54) in the interface portion (A slot 500 is an abstraction that may have a bump/bond pad area 510, an I/O area 520, and/or an edge logic area 530 – col.7, ll.57-59; logic area 530 is an area for placing standard cells that need to be placed close to the corresponding I/O cell to satisfy timing constraints – col.8, ll.1-3) (col.6, ll.59-67; col.7, ll.1-2; col.7, ll.56-67; col.8, ll.1-9; col.14, ll.49-61); and

an interface definition comprising a plurality of source-synchronous interface I0 signal nets including a multiple-bit data bus and a first clock strobe net, wherein signals on the data bus have a desired phase alignment with respect to signals on the first clock strobe net(At Block 350, a final customization of the padring layout design is performed. This final customization can include, for example, laying down special escape pattern cover cells and adding prerouted wires near the edge logic areas to provide a bus with shielding for low skew balanced buses. This is useful for source-synchronous buses where consistent loading on the data and clock lines is important to achieve a low skew specification –col.18, ll.13-20), wherein the nets are routed to corresponding ones of the plurality of macro cell signal slots (For cases where the routing in the edge logic area is to be controlled also, the third placement algorithm is used. Here, a macro is constructed (such that the edge logic is placed and routed) and placed in each edge

logic area to guarantee absolute consistency between related edge logic areas –col.18, ll.7-12), and wherein the macro cell is adapted to be instantiated as a unit in the integrated circuit design (Through an instantiation process, the slots 500 are created by using the pattern over and over again in the padring area. The instantiation of slots 500 is what fixes their bump/bond pad area 510, I/O area 520, and edge logic area 530 to a specific position on the padring area of the chip col.8, ll.23-27) (col.8, ll.23-31; col.17, ll.59-67; col.18, ll.1-20);

(8) A macro cell for instantiation in an integrated circuit design, the macro cell comprising:

a physical layer interface definition comprising a multiple-bit data bus and a first clock strobe net, wherein signals on the data bus have a desired phase alignment with respect to signals on the clock strobe net (col.6, ll.59-67; col.7, ll.1-2; col.7, ll.56-67; col.8, ll.1-9; col.14, ll.7-21; col.14, ll.49-61; col.15, ll.45-60; col.18, ll.13-21); and

a plurality of macro cell input-output (I0) slots, which are electrically coupled to respective bits in the multiple-bit data bus and the first clock strobe net and are physically dispersed from one another in a spacing pattern that is defined for at least one integrated circuit package type, wherein the macro cell is adapted to be instantiated in the integrated circuit design as a unit (col.8, ll.23-31; col.15, ll.45-67; col.16, ll.1-12; col.17, ll.59-67; col.18, ll.1-20);

(17) An integrated circuit layout definition comprising:

an input-output (I0) region comprising an interface portion and a plurality of I0 buffer cells physically dispersed with other cells in I0 slots along the interface portion (col.7, ll.56-67; col.8, ll.1-9); and

a macro cell instantiated in the layout definition and comprising:

a plurality of macro cell I0 signal slots that are physically dispersed so as to substantially align with corresponding ones of the I0 buffer cells in the interface portion (col.6, ll.59-67; col.7, ll.1-2; col.7, ll.56-67; col.8, ll.1-9; col.14, ll.49-61); and

an interface definition comprising a plurality of source-synchronous interface I0 signal nets, which are routed to corresponding ones of the plurality of macro cell signal slots and include a multiple-bit data bus and a clock strobe net, wherein signals on the data bus have a desired phase alignment with respect to signals on the clock strobe net (col.8, ll.23-31; col.17, ll.59-67; col.18, ll.1-20).

4. As to claims 2, 7, 9-12 and 18 Dahl recites:

(2), (12) The macro, wherein the macro cell I0 signal slots are dispersed among other, unused I0 slots within the macro cell (col.6, ll.59-67; col.7, ll.1-2; col.7, ll.56-67; col.8, ll.1-9; col.14, ll.49-61; col.15, ll.25-44);

(7), (11), (18) The macro cell, wherein the plurality of I0 buffer cells is physically dispersed with power supply cells (col.10, ll.43-57; col.15, ll.25-44);

(9), (10) The macro cell, the spacing pattern is defined for a plurality of different integrated circuit package types (col.15, ll.62-67; col.16, ll.1-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-4, 6, 13-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dahl in view of Davidson et al. (US Patent 6,894,530).

With respect to claims 3-4, 6, 13-14 and 16 Dahl teaches the features above but lacks an integrated circuit layout definition, wherein the physical layer interface definition defines circuitry adapted to transfer data over the data bus at a first data rate with every other transition on the first clock strobe net and at a second, faster data rate with each transition on the first clock strobe net.

6. As to claim claims 3-4, 6, 13-14 and 16 Davidson teaches:

(3), (4), (6), (13), (14) The macro cell, wherein the physical layer interface definition defines circuitry adapted to transfer data over the data bus at a first data rate with every other transition on the first clock strobe net and at a second, faster data rate with each transition on the first clock strobe net (Abstract; col.2, ll.9-31; col.8, ll.3-34).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Davidson's teaching regarding the integrated circuit layout definition, wherein the physical layer interface definition defines circuitry adapted to transfer data over the data bus at a first data rate with every other transition on the first clock strobe net and at a second, faster data rate with each transition on the first

clock strobe net to improve the synchronization of the transferred data using, for example, single data rate (SSD) and double data rate (DDR), thereby decreasing the size of the data bus.

Allowable Subject Matter

7. Claims 5 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

The macro cell of claim 3 (8), wherein each bit of the multiple-bit data bus comprises a transmit bit, a receive bit and an enable bit; and the respective macro cell I0 signal slot for each of bit of the data bus defines physical pin locations for the transmit bit, receive bit and enable bit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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THUAN DO
Primary examiner.
05/04/2006